CHW 261: Logic Design

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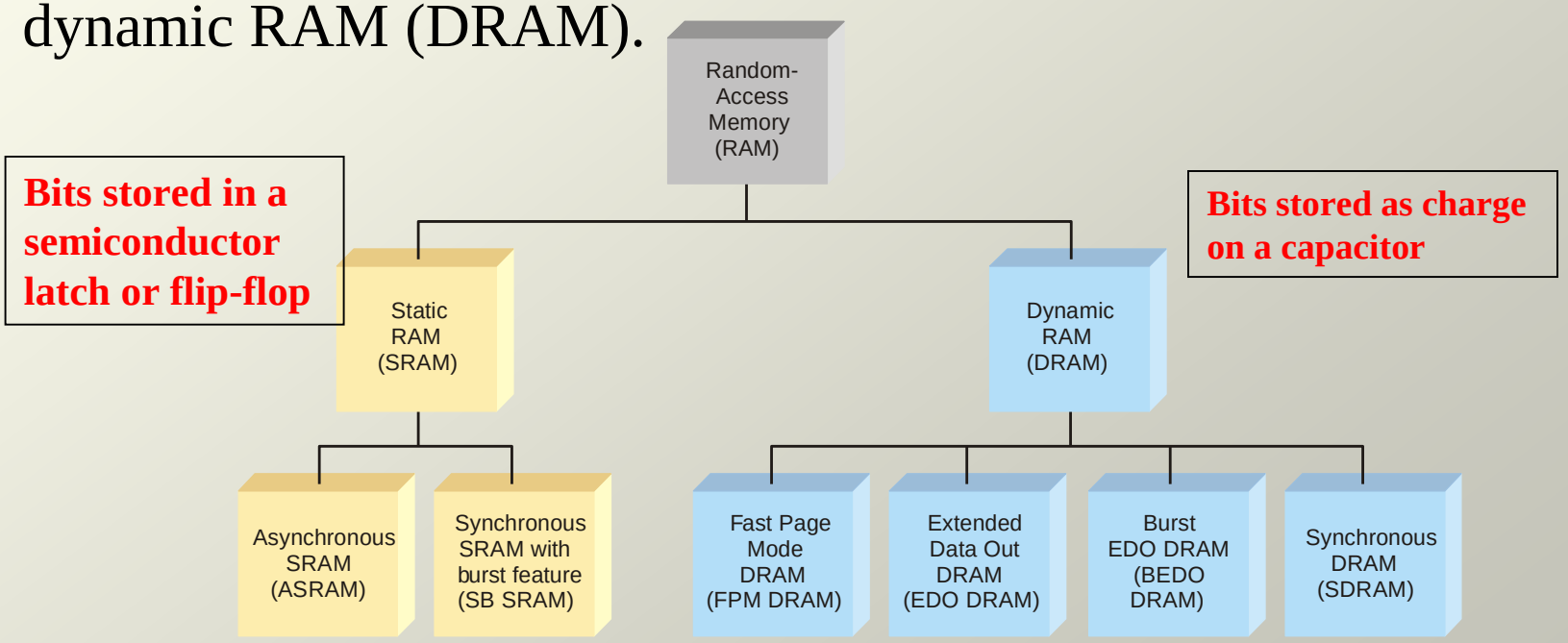
Digital Fundamentals

Applications

Applications

Random Access Memory

RAM is for temporary data storage. It is read/write memory and can store data only when power is applied, hence it is *volatile*. Two categories are static RAM (SRAM) and dynamic RAM (DRAM).



Applications

Memory Units

Memories store data in units from one to eight bits. The most common unit is the **byte**, which by definition is 8 bits.

Computer memories are organized into multiples of bytes called words. Generally, a word is defined as the number of bits handled as one entity by a computer. By this definition, a word is equal to the internal register size (usually 16, 32, or 64 bits).

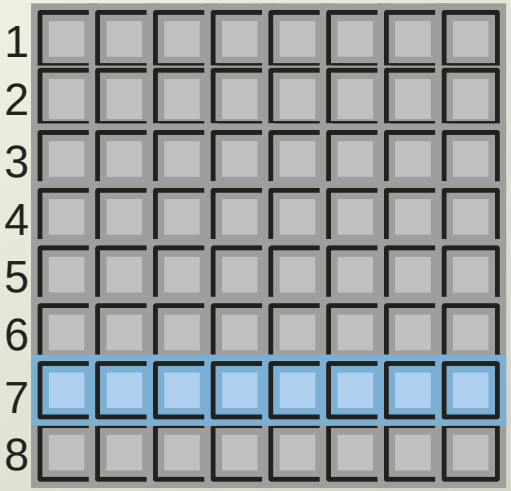
For historical reasons, assembly language defines a word as exactly two bytes. In assembly language, a 32 bit entity is called a double-word and 64 bits is defined as a quad-word.

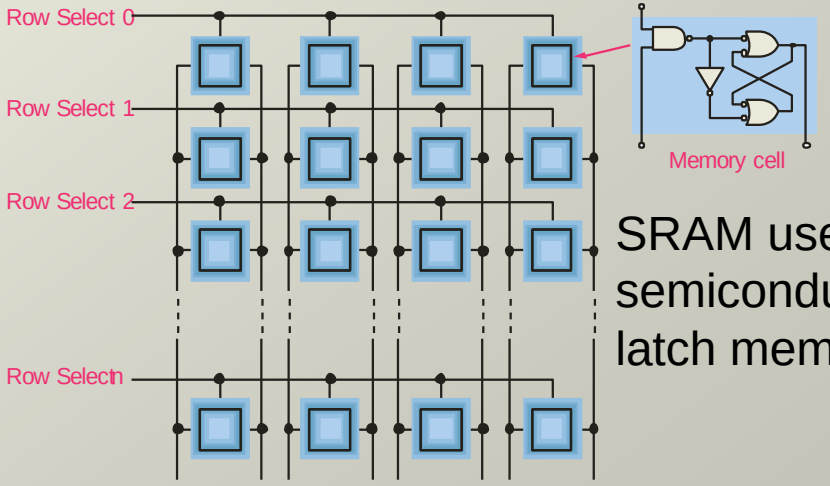
Applications

Memory Units

The location of a unit of data in a memory is called the **address**. In PCs, a byte is the smallest unit of data that can be accessed.

In a 2-dimensional array, a byte is accessed by supplying a row number. For example the blue byte is located in row 7.





SRAM uses semiconductor latch memory cells

Applications

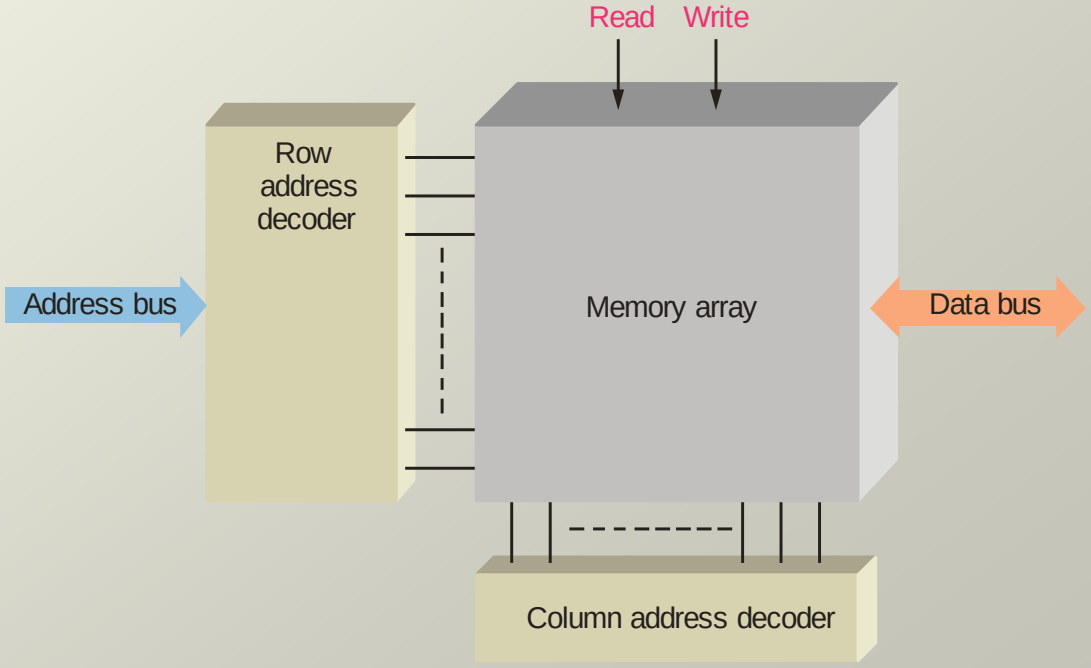
Memory Addressing

In order to read or write to a specific memory location, a binary code is placed on the **address bus**.

Internal decoders decode the address to determine the specific location. Data is then moved to or from the **data bus**.

The address bus is a group of conductors with a common function.

Its size determines the number of locations that can be accessed. A 32 bit address bus can access 2^{32} locations, which is approximately 4G.



Applications

Memory Addressing

In addition to the address bus and data bus, semiconductor memories have read and write control signals and chip select signals. Depending on the type of memory, other signals may be required.

Read Enable ($\overline{RE}$) and **Write Enable** ($\overline{WE}$) signals are sent from the CPU to memory to control data transfer to or from memory.

Chip Select ($\overline{CS}$) or **Chip Enable** ($\overline{CE}$) is used as part of address decoding. All other inputs are ignored if the Chip Select is not active.

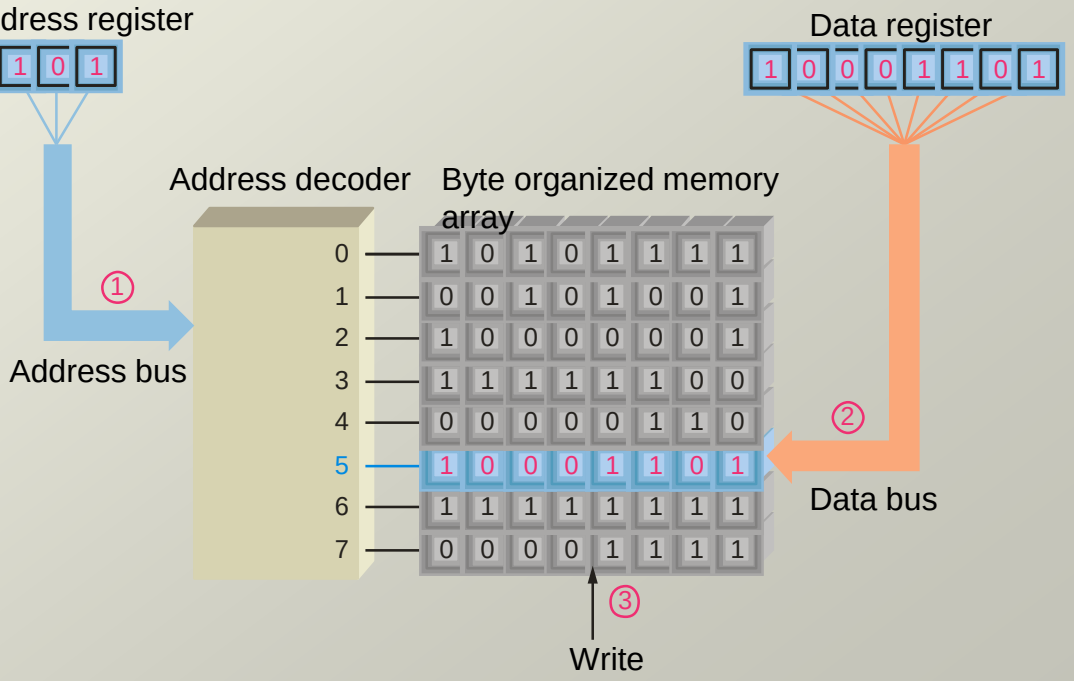
Output Enable ($\overline{OE}$) is active during a read operation, otherwise it is inactive. It connects the memory to the data bus.

Applications

Write Operation

The two main memory operations are called **read** and **write**. A simplified write operation is shown in which new data overwrites the original data. Data moves *to* the memory.

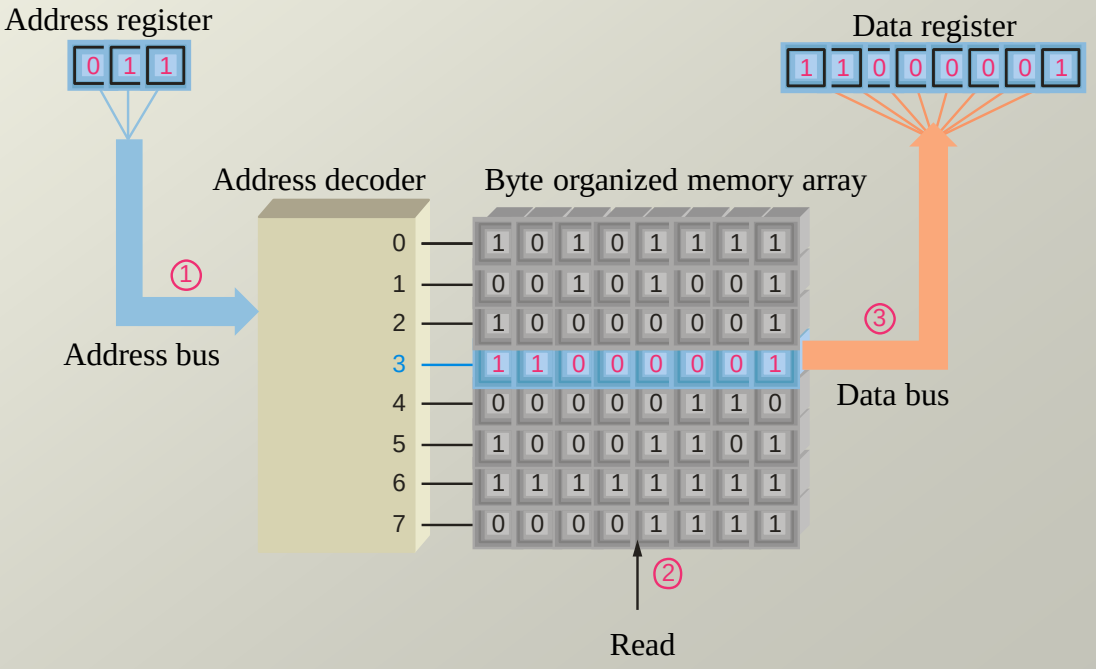
1. The address is placed on the address bus.
2. Data is placed on the data bus.
3. A write command is issued.



Applications

Read Operation

The read operation is actually a “copy” operation, as the original data is not changed. The data bus is a “two-way” path; data moves *from* the memory during a read operation.

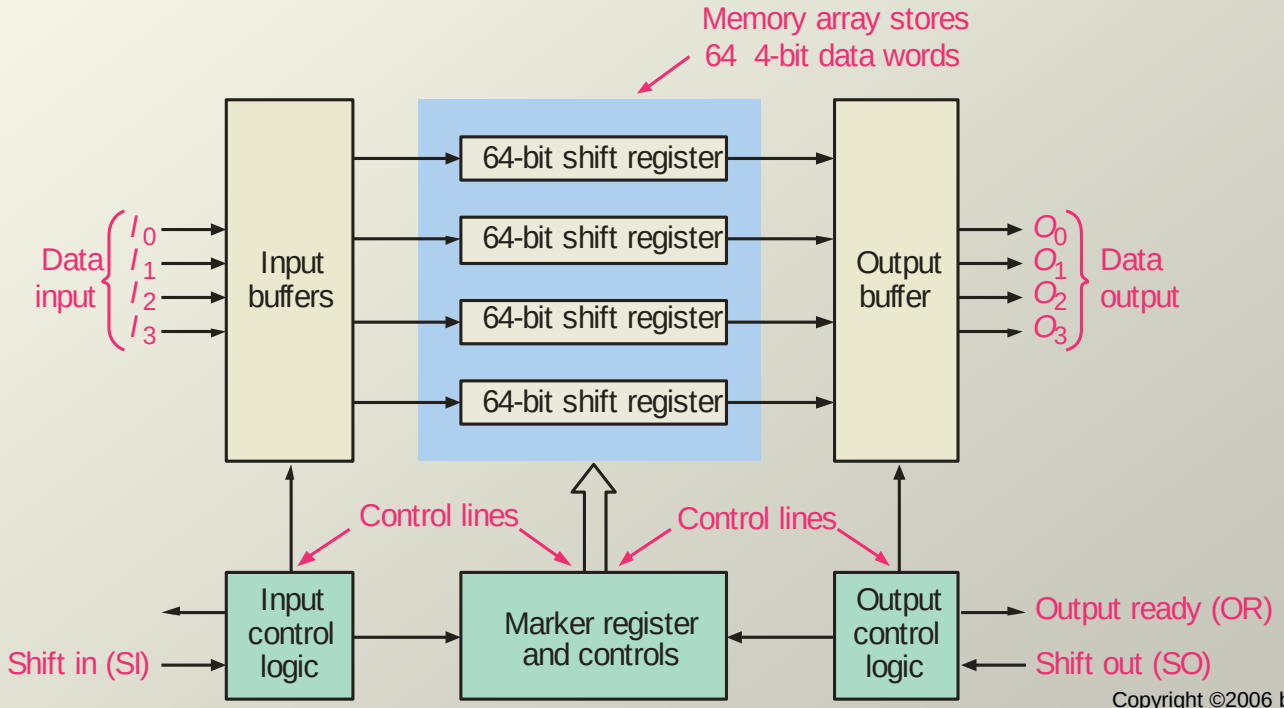


1. The address is placed on the address bus.
2. A read command is issued.
3. A copy of the data is placed in the data bus and shifted into the data register.

Applications

FIFO Memory

FIFO means first in-first out. This type of memory is basically an arrangement of shift registers. It is used in applications where two systems communicate at different rates.



Applications

Programmable Logic

Programmable Logic Devices (PLDs) are ICs with a large number of gates and flip flops that can be configured with basic software to perform a specific logic function or perform the logic for a complex circuit. Major types of PLDs are:

SPLD: (Simple PLDs) are the earliest type of array logic used for fixed functions and smaller circuits with a limited number of gates. (**The PAL and GAL are both SPLDs**).

CPLD: (Complex PLDs) are multiple SPLDs arrays and inter-connection arrays on a single chip.

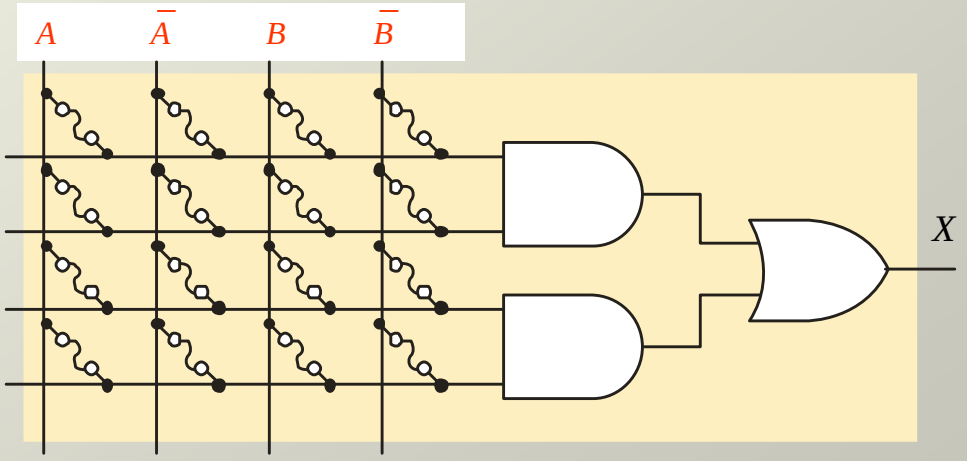
FPGA: (Field Programmable Gate Array) are a more flexible arrangement than CPLDs, with much larger capacity.

Applications

PALs and GALs

All PLDs contain arrays. Two important SPLDs are **PALs** (Programmable Array Logic) and **GALs** (Generic Array Logic). A typical array consists of a matrix of conductors connected in rows and columns to AND gates.

PALs have a one time programmable (OTP) array, in which fuses are permanently blown, creating the product terms in an AND array.



Simplified AND-OR array

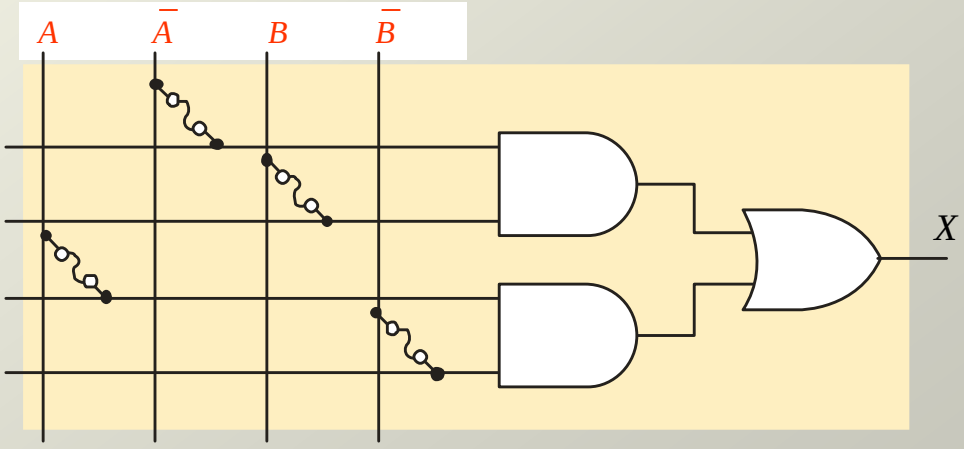
Applications

PALs and GALs

PALs are programmed with a specialized programmer that blows selected internal fuse links. After blowing the fuses, the array represents the Boolean logic expression for the desired circuit.

Example

What function is represented by the array?



Solution $X = \overline{A}B + A\overline{B}$

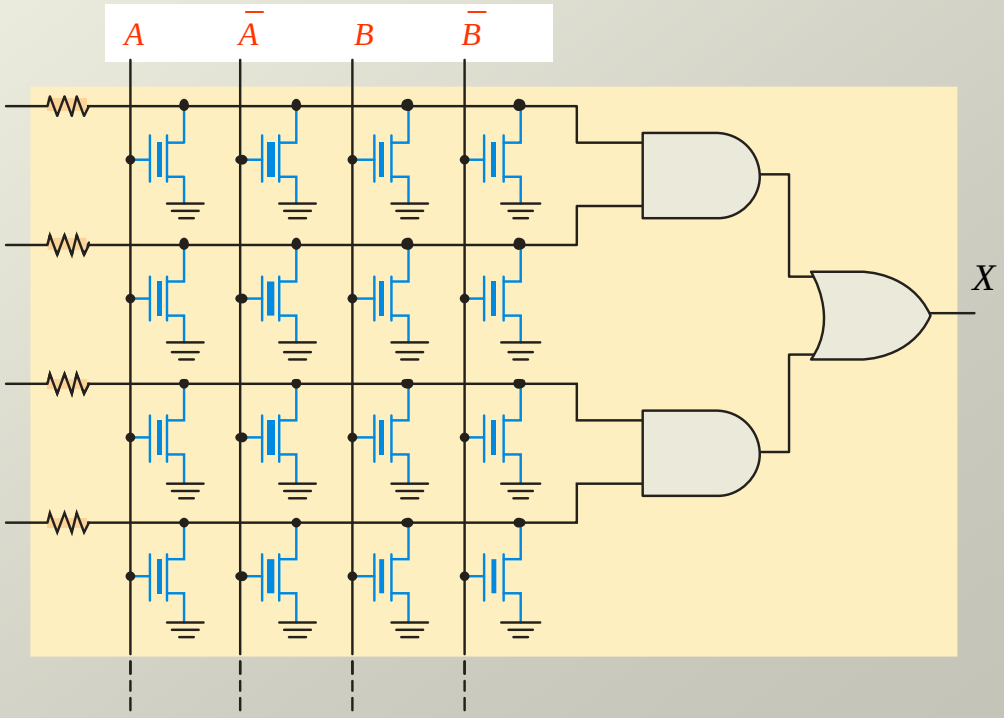
The function represents an XOR gate.

Applications

PALs and GALs

The GAL (Generic Array Logic) is similar to a PAL but can be reprogrammed. For this reason, they are useful for new product development (prototyping) and for training purposes.

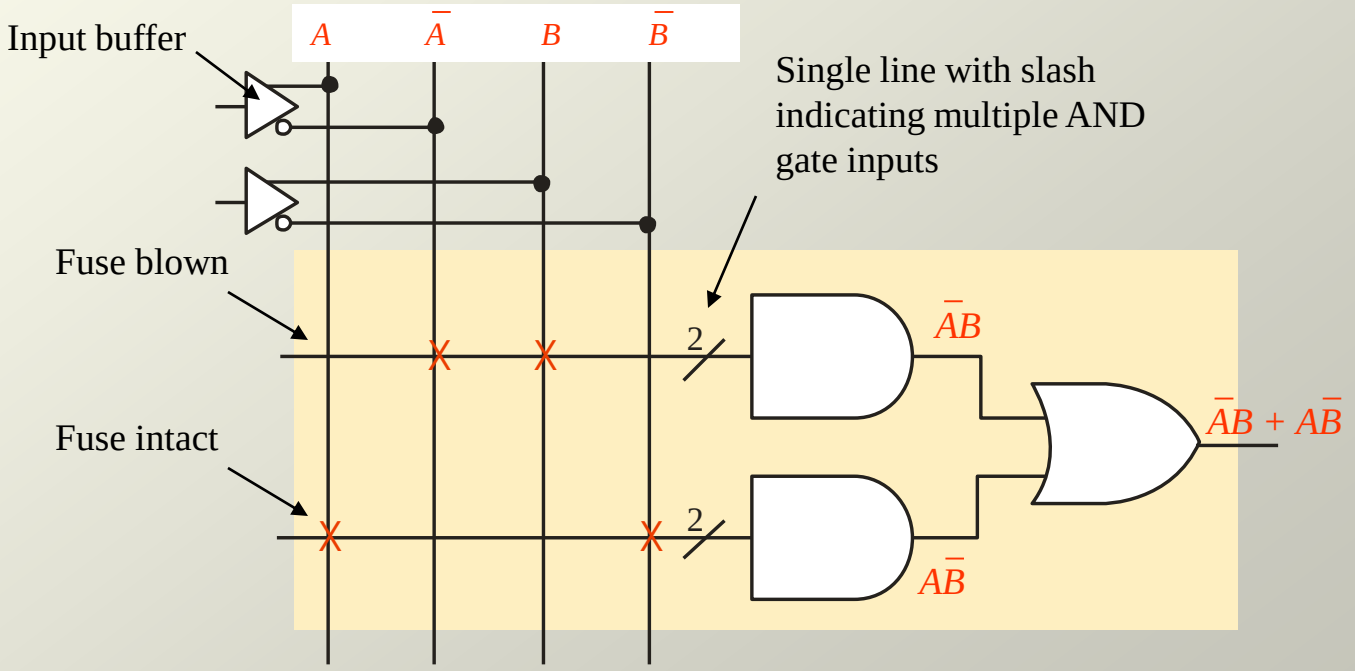
GALs were developed by Lattice Semiconductor. They are high speed, extremely fast devices and can interface with both 3.3 V or 5 V logic signals.



Applications

PALs and GALs

PALs and GALs can be represented with a simplified diagram. A single line can represent multiple gate inputs. The logic shown is for the XOR gate, given previously.

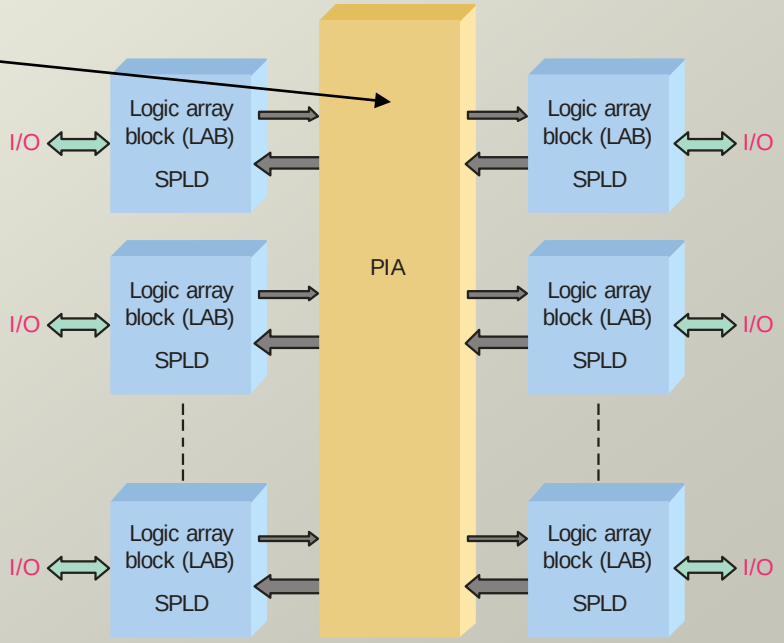


Applications

CPLDs

A complex programmable logic device (**CPLD**) has multiple logic array blocks (**LAB**s) that are actually SPLDs on a single IC. LABs are connected via a programmable interconnect array (**PIA**). Various CPLDs have different structures for these elements.

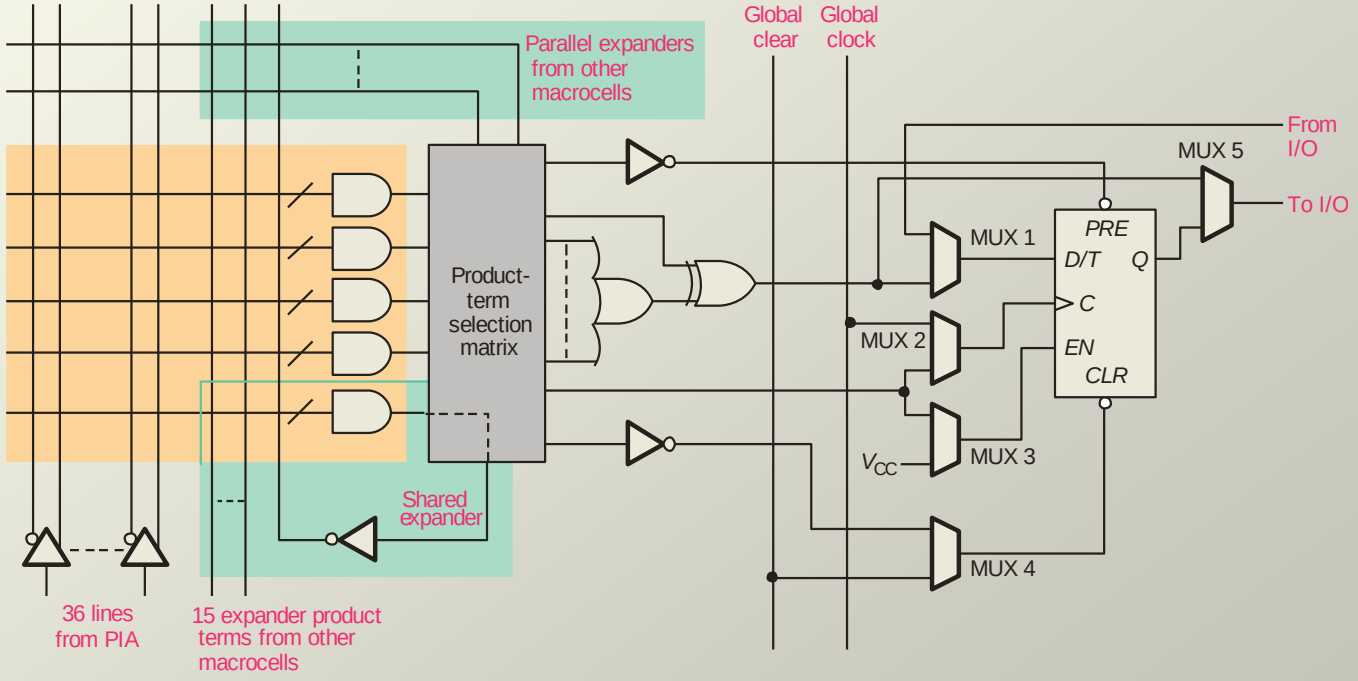
The PIA is the interconnection between the LABs. Logic is fitted to the CPLD and routing is determined by a high-level programming language called a hardware description language (HDL).



Applications

Macrocells

In addition to combination logic, some **macrocells** have registered outputs available (using programmable flip-flops). This allows the CPLD to perform sequential logic.

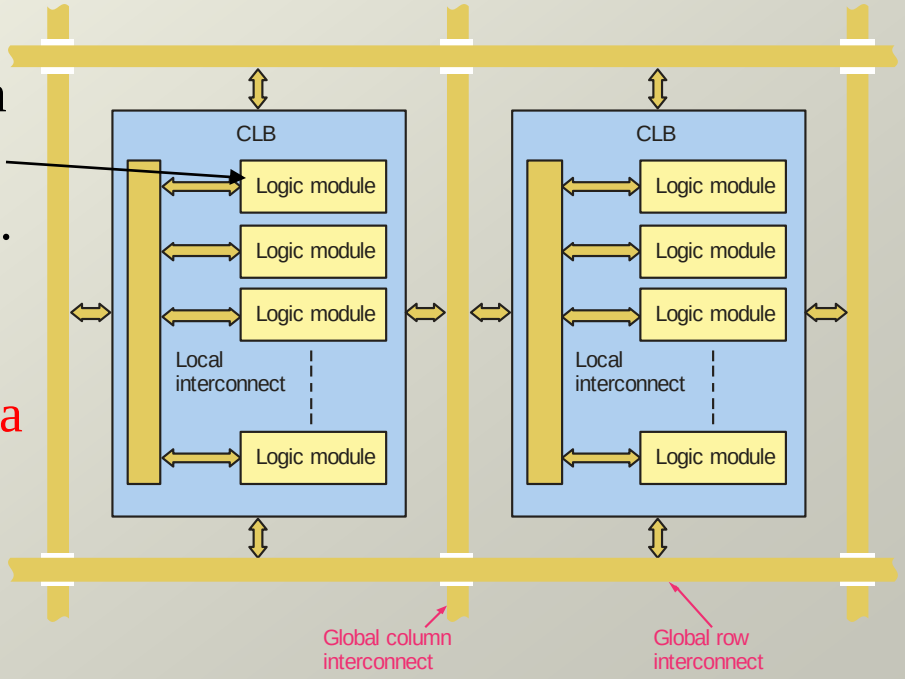


Applications

FPGAs

A field programmable gate array (**FPGA**) uses a different architecture than a CPLD. The configurable logic block (**CLB**) is the basic element which is replicated many times.

CLBs are arranged in a row and column structure. Within the CLBs are **logic modules** joined by local interconnects. Generally, the logic modules are composed of a look-up table (LUT), a flip-flop, and a MUX that can be used to bypass the flip-flop for strictly combinational logic.



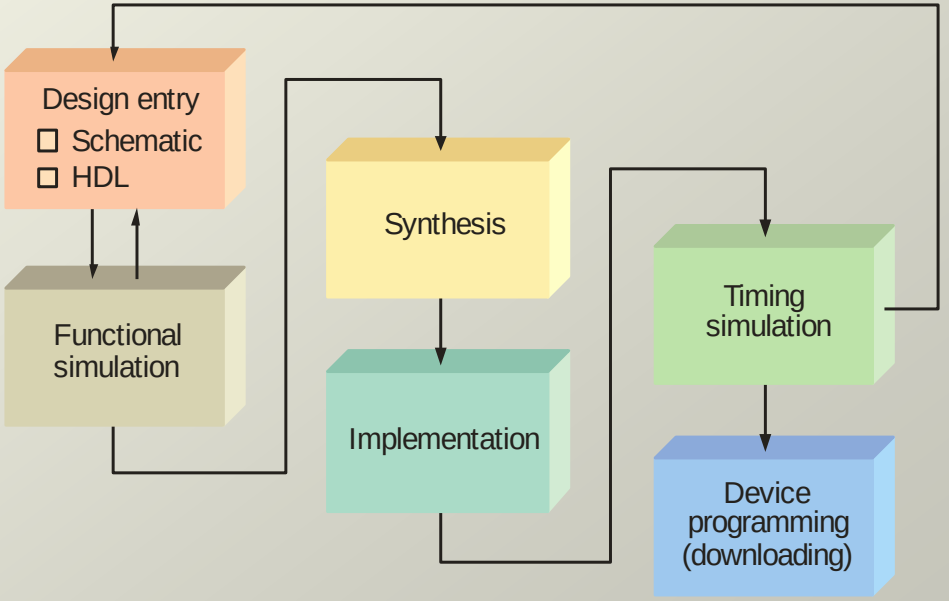
Applications

Programmable Logic Software

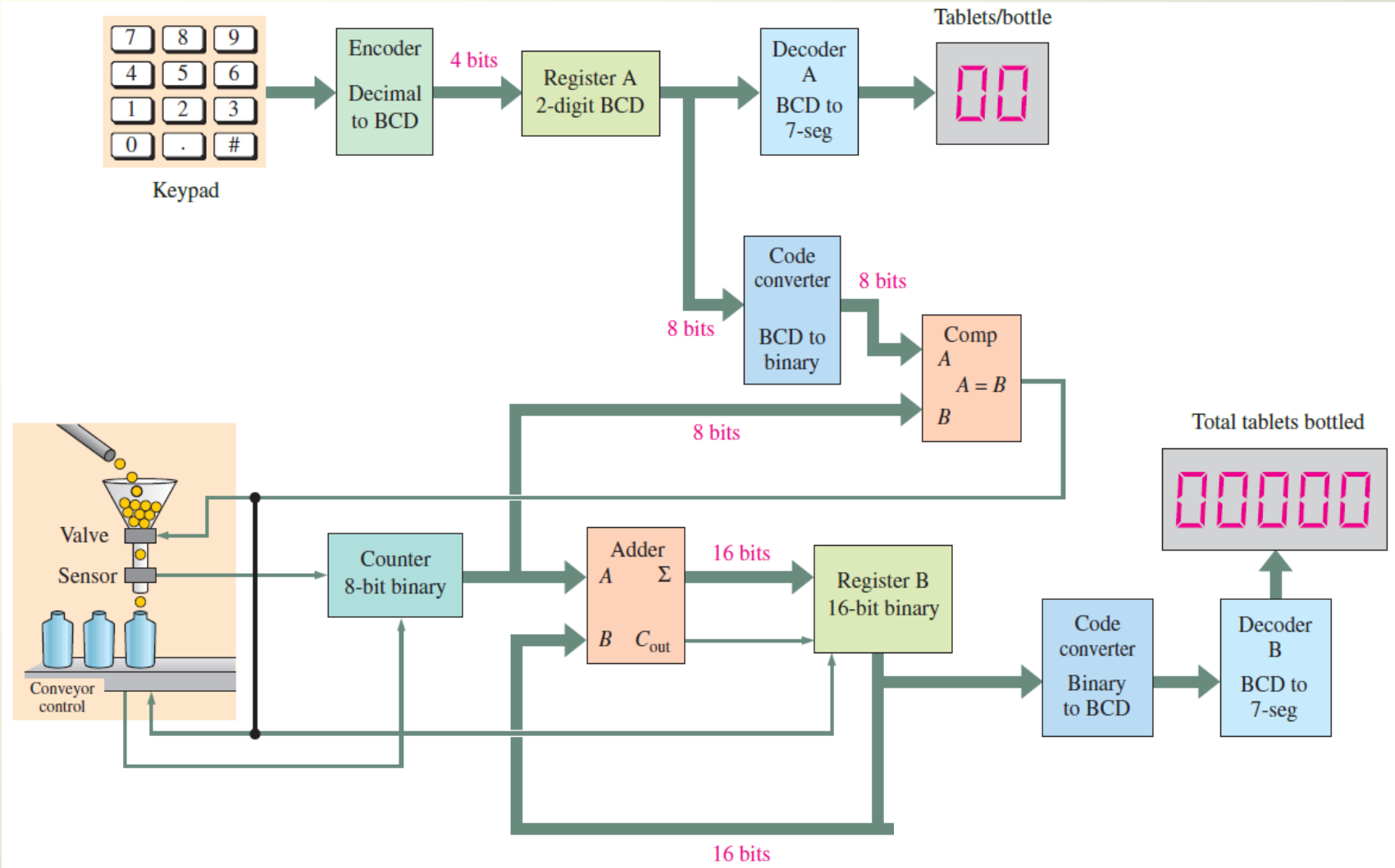
All manufacturers of programmable logic provide software to support their products. The process is illustrated in the flowchart.

The first step is to enter the logic design into a computer. It is done in one of two ways:

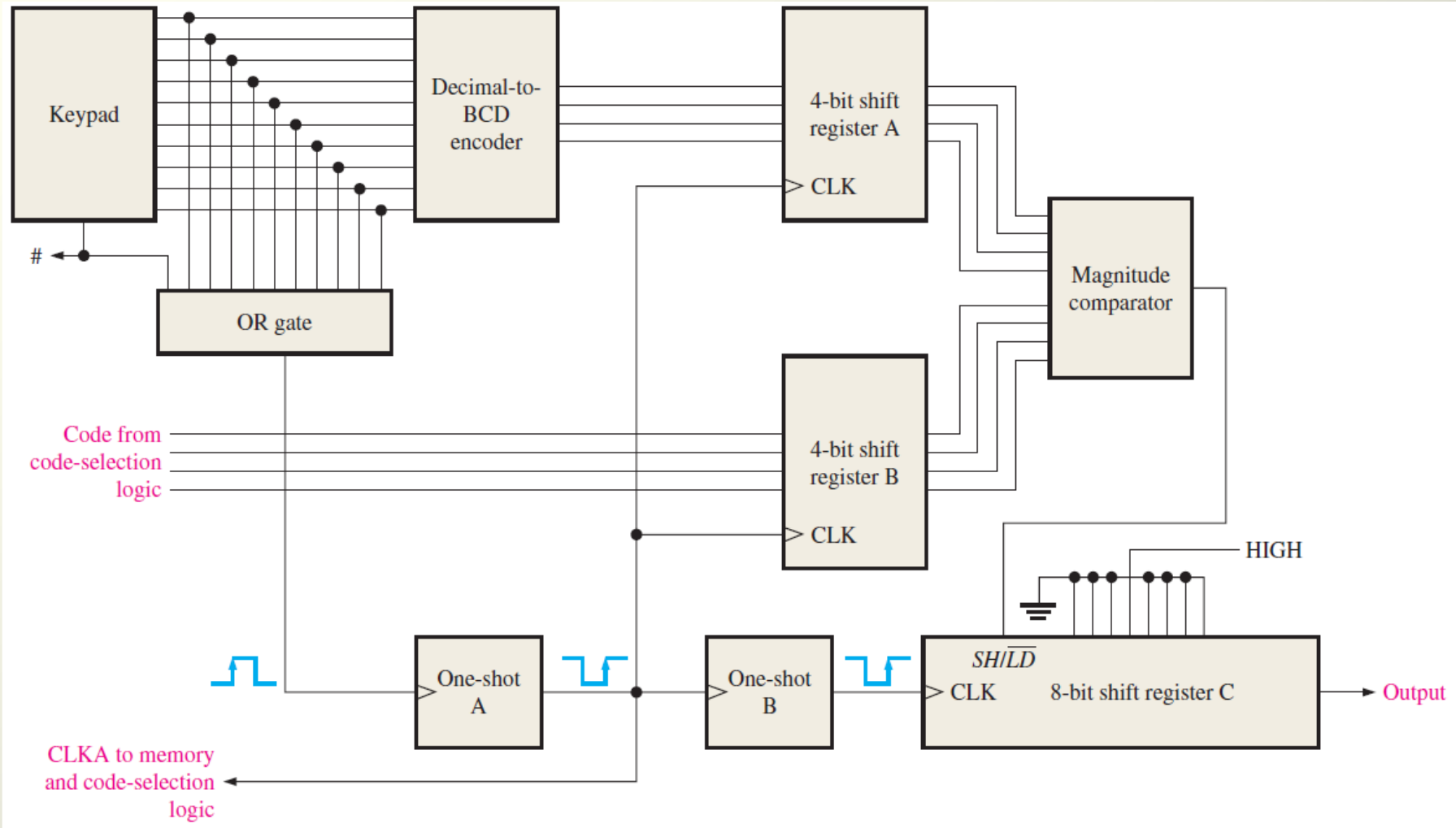
1) Schematic entry
2) Hardware description language (HDL).



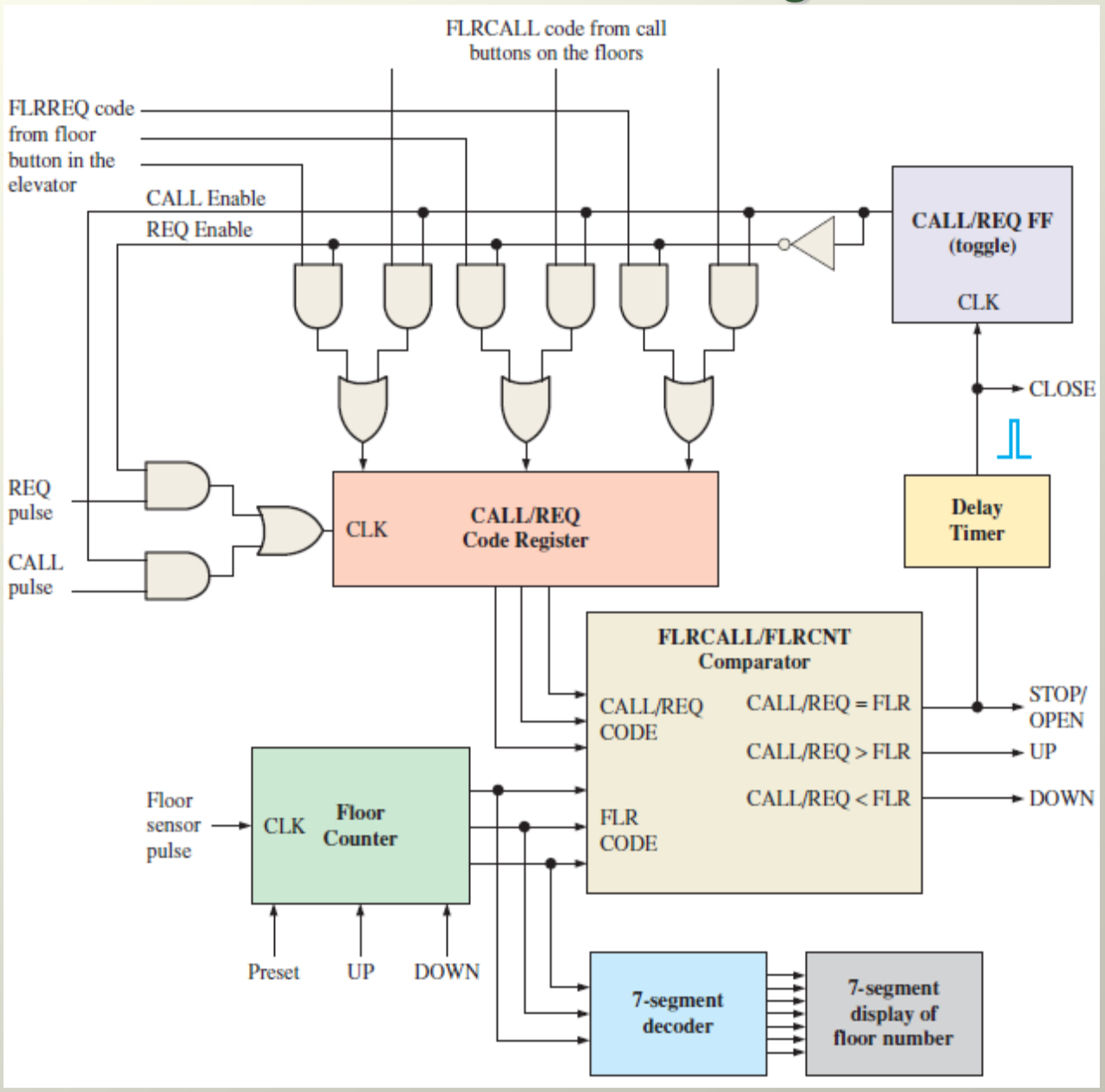
Applications : Tablet-bottling System



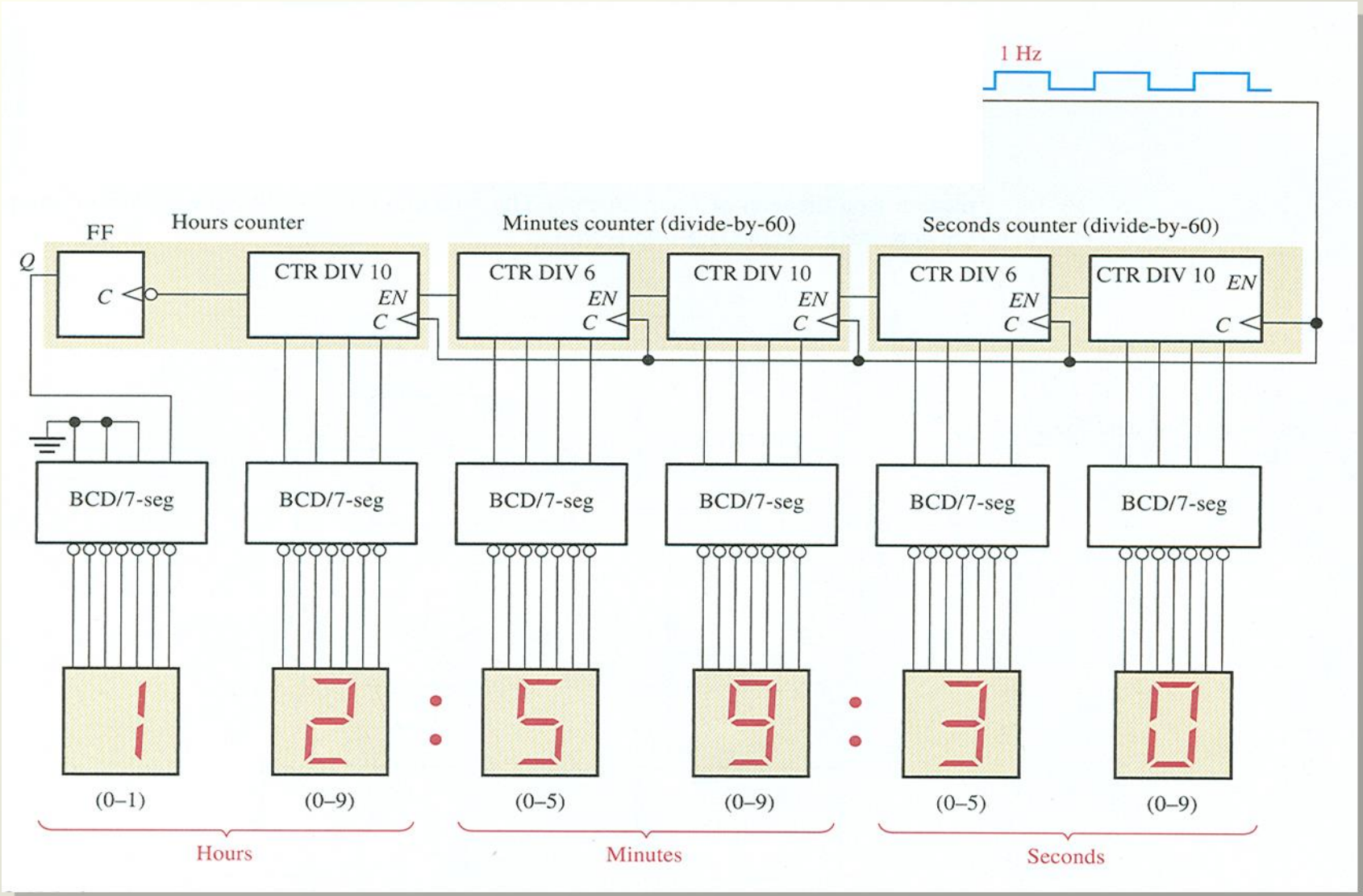
Applications: Security Code Logic with Keypad



Applications : Elevator controller logic



Applications : Digital Clock



Applications : Traffic Light Controller